Crystal Bridge to the Future

Real Time Clock Module

Application Manual

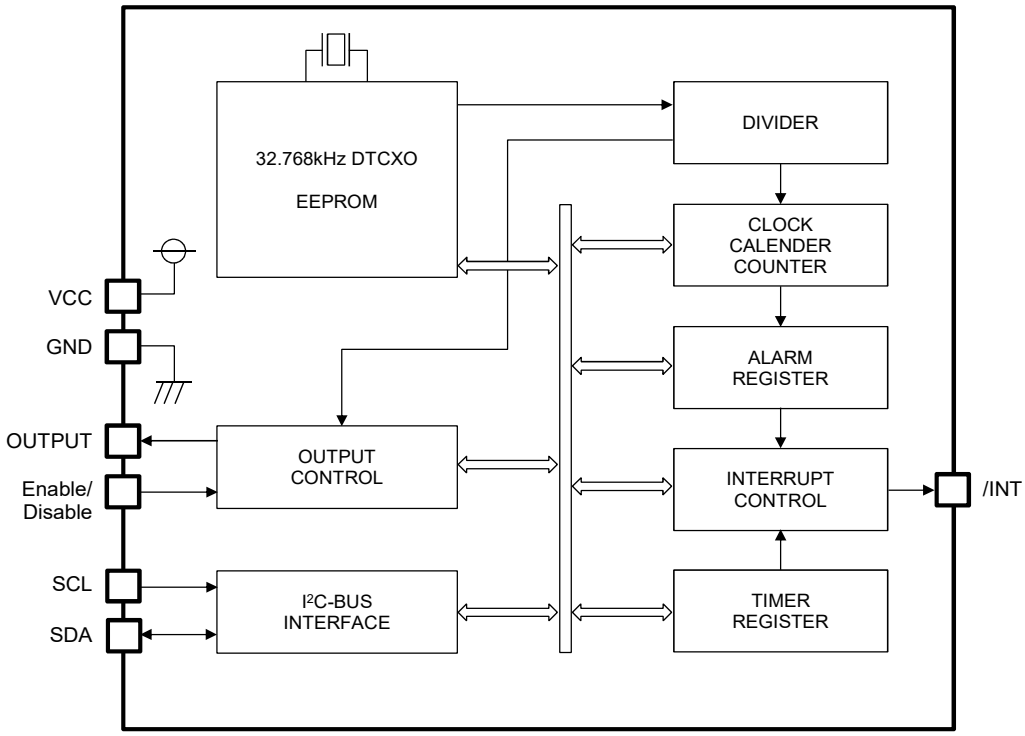
Instruction manual: ETS95B-00001
NIHON DEMPA KOGYO CO., LTD.

Contents

1. Overview

This product is a high stability real time clock module of the I^2C-BUS interface system which built in 32.768kHz DTCXO.In addition to the clock and the calendar function, this module have an alarm interruption function,the constant cycle timer interruption function, the time update interruption function, the clock output function, and the power supply voltage detection function.

2. Block Diagram



3. Terminal Functions

Terminal Name	I/0	Function
Enable /Disable	I	This terminal an input pin used OUTPUT terminal.When this terminal's level is high, the output terminal is output mode.When it is low, the output terminal is ‘’Hi-Z” (High Impedance).
/INT	I	Outputs for alarm signals, timer signals timer update signals and other signals. This terminal is an open drain terminal.
GND	-	Connected to a ground.
OUTPUT	0	32.768kHz signal output (CMOS output)
SCL	I	Serial clock input for I_2C-BUS communications.
SDA	I/0	Serial data input output for I_2C-BUS communications.This terminal inputs and outputs address, data and acknowledge bit in synchronized with SCL clock input by the Nch open drain output.
VCC	-	This pin is connected to a positive power supply

4. Maximum Rating

Item	Symbol	Terminal	Condition	Unit
Supply Voltage	V_{CC}	V_{CC}	-0.3 to +6.5	V
Input Voltage *1	V_{IN}	SCL,SDA,E/D	-0.3 to +6.5	V
Output Voltage *1,*2	V_{OUT1}	OUTPUT	-0.3 to V_{CC}+0.3	V
	V_{OUT2}	SDA,/INT	-0.3 to +6.5	V
Storage temp. range *3	T_{STG}	-	-40 to +105	°C

*1 It is a value which must not exceed even a moment. If it should exceed, there is concern of destruction of IC, characteristic degradation, and a reliability fall.

*2 It is a value which V_{CC} value is a V_{CC} value of recommendation operation power supply voltage.

5. Electrical Characteristics

5-1. AC characteristics (I_2C-BUS serial interface: Clock control register access)

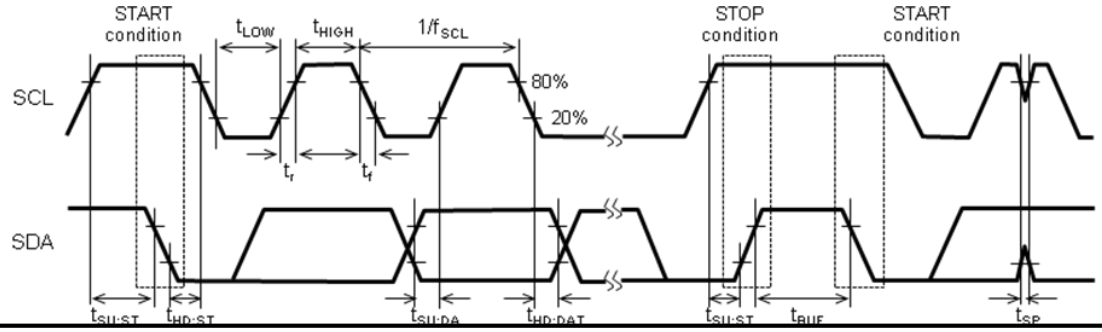
V_{CC} = 1.5 to 5.5V , GND=0V , Ta=-40 to +105°C

Parameter	Symbol	Condition	Spec			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	-	-	-	400	kHz
Start condition setup time	$t_{SU,STA}$	-	0.6	-	-	µs
Start condition hold time	$t_{HD,STA}$	-	0.6	-	-	µs
Data setup time	$t_{SU,DAT}$	-	100	-	-	ns
Data hold time	$t_{HD,DAT}$	-	0	-	900	ns
Stop condition setup time	$t_{SU,STO}$	-	0.6	-	-	µs
Bus free time between start and stop conditions	t_{BUF}	-	1.3	-	-	µs
SCL "L" puls time	t_{LOW}	-	1.3	-	-	µs
SCL "H" puls time	t_{HIGH}	-	0.6	-	-	µs
SCL,SDA fise time	tr	20% -> 80%	-	-	0.3	µs
SCL,SDA fall time	tf	80% -> 20%	-	-	0.3	µs
Maximum bus spike time	t_{SP}	-	-	-	50	ns
Bus line load capacitancee	C_b	Vcc ≥ 1.8V	-	-	400	pF
		Vcc < 1.8V	-	-	50	pF

Note.

This RTC module access from the transfer of the start condition until the stop condition should be completed within 0.5 seconds.If the access exceeds 0.5 seconds, an internal monitor timer forcibly terminates the RTC bus interface access.

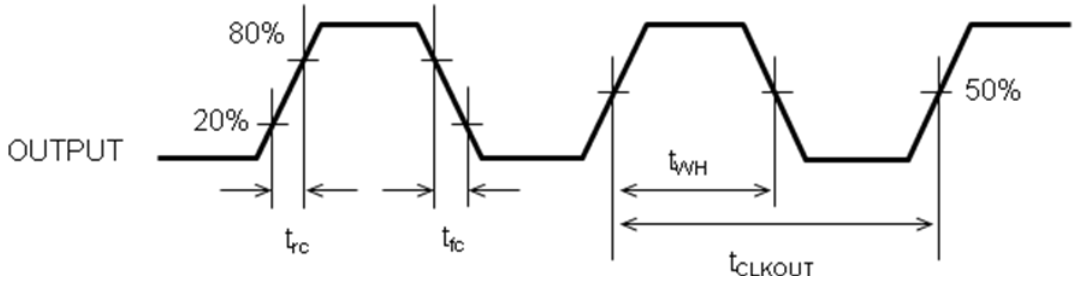
Timing Chart



5-2. AC characteristics (OUTPUT terminal)

V_{CC} = 1.5 to 5.5V , GND=0V , Ta=-40 to +105℃

Parameter	Symbol	Conditions		Spec			Unit
				Min.	Typ.	Max.	
OUTPUT Duty	Duty	C_{LOUT}=15pF , threshold 0.5V_{CC} threshold		40	50	60	%
OUTPUT rise time	t_{rC}	C_{LOUT}=15pF 20% → 80%	Vcc=1.8 to 5.5V	-	-	70	ns
			Vcc=1.5 to 5.5V	-	-	180	ns
			Vcc=1.3 to 5.5V	-	-	1100	ns
OUTPUT fall time	t_{fC}	C_{LOUT}=15pF 80% → 20%	Vcc=1.8 to 5.5V	-	-	70	ns
			Vcc=1.5 to 5.5V	-	-	180	ns
			Vcc=1.3 to 5.5V	-	-	1100	ns

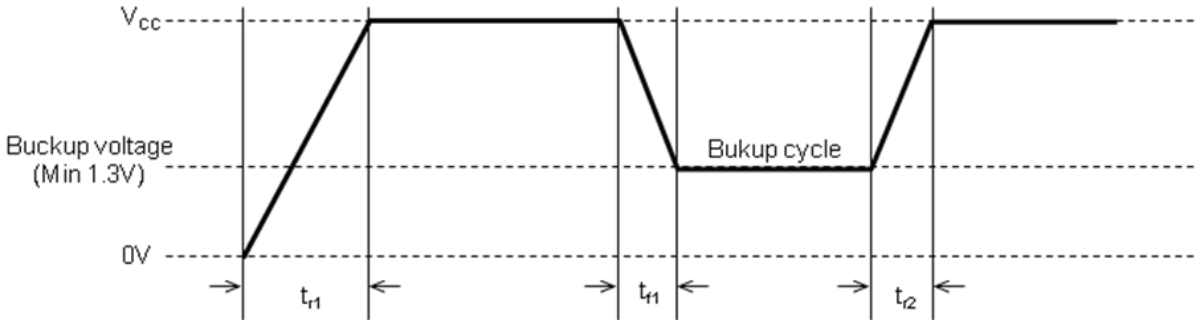


Duty = t_{WH} / t_{OUTPUT} x 100(%)

5-3. Power Supply Rise Time and Fall Time

Paramete	Symbol	Conditions	Spec			Unit
			Min.	Typ.	Max.	
Startup supply voltage rise time	t_{r1}	-	-	-	10	ms/V
Backup transition supply voltage fall time	t	-	5	-	-	μs/V
Backup return supply voltage rise time	t_{r2}	-	5	-	-	μs/V

This device is equipped with a power-on reset circuit to initialize internal settings when power is first applied. If supply voltage rise time or fall time are outside the specified time, there is a possibility that the power on reset circuit may not be activated when power is first applied or during the backup transition/return cycle. Ensure supply voltage rise times and fall times are within the specified values for stable, correct, power-on reset circuit operation.



6. Description of functions

6-1. Time Control Register Table

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00h	SEC	-	S40	S20	S10	S8	S4	S2	S1
01h	MIN	-	M40	M20	M10	M8	M4	M2	M1
02h	HOUR	-	-	H20	H10	H8	H4	H2	H1
03h	WEEK	-	-	-	-	-	W4	W2	W1
04h	DAY	-	-	D20	D10	D8	D4	D2	D1
05h	MONTH	-	-	-	MO10	MO8	MO4	MO2	MO1
06h	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07h	MIN Alarm	AE	MA40	MA20	MA10	MA8	MA4	MA2	MA1
08h	HOUR Alarm	AE	RAM	HA20	HA10	HA8	HA4	HA2	HA1
09h	WEEK Alarm	AE	WA6	WA5	WA4	WA3	WA2	WA1	WA0
	DAY Alarm		RAM	DA20	DA10	DA8	DA4	DA2	DA1
0Ah	Timer Counter	T128	T64	T32	T16	T8	T4	T2	T1
0Bh	Select Register	TCS1	TCS0	CFS1	CFS0	TSS1	TSS0	AS	UTS
0Ch	Flag Register	-	-	VDHF	VDLF	-	TF	AF	UTF
0Dh	Control Register	RESET	TEST	RAM	FIE	TE	TIE	AIE	UTIE

* The register values are undefined when power is first applied; ensure the device is configured before use. Note that the TCS1, TCS0, CFS1, CFS0, TEST, FIE, TE, TIE, AIE, and UTIE bits are reset to “0”, and the VDLF bit is set to “1” when power is applied.
* Bits indicated by a hyphen ”-” are read-only bits with read output value of “0”.
* Only “0” data values can be written to the VDHF, VDLF, TF, AF, and UTF bits.
* The TEST bit is a reserved bit for manufacturer testing, and should always be set to “0” for normal operation.
* Bexause the write-in read-out operation to Address 0Eh and 0Fh causes malfunction, it is considered as an access inhibit.

6-2. Time and Calendar Register (Address 00h – Address 06h)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00h	SEC	-	S40	S20	S10	S8	S4	S2	S1
01h	MIN	-	M40	M20	M10	M8	M4	M2	M1
02h	HOUR	-	-	H20	H10	H8	H4	H2	H1
03h	WEEK	-	-	-	-	-	W4	W2	W1
04h	DAY	-	-	D20	D10	D8	D4	D2	D1
05h	MONTH	-	-	-	MO10	MO8	MO4	MO2	MO1
06h	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

•Data format
The time and calendar data is couched in BCD format.

•HOUR register
The HOUR register contains the hour in 24-hour display mode.

•WEEK register
The WEEK register increments using a 7-step up-counter (W4W2W1)=(000)→(001)→…→(110)→ (000).
The logic table for the (W4W2W1) bits for the day of the week are configurable by the user.

•YEAR register
The YEAR register contains the last 2 digits of the western calendar year.

•Automatic leap year correction function
The automatic leap year correction function corrects for leap years between 2000 and 2099.

•Example time and calendar setting
For a time of 5:43:21 in the morning on Sunday, July6, '98
(Assuming the WEEK register setting for Sunday = (W4W2W1) = (000))

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00h	SEC	-	0	1	0	0	0	0	1
01h	MIN	-	1	0	0	0	0	1	1
02h	HOUR	-	-	0	0	0	1	0	1
03h	WEEK	-	-	-	-	-	0	0	0
04h	DAY	-	-	0	0	0	1	1	0
05h	MONTH	-	-	-	0	0	1	1	1
06h	YEAR	1	0	0	1	1	0	0	0

* Time and calendar setting that are invalid will result in malfunction. Always ensure the data settings are valid.

6-3. Alarm Registers (Address 07h – Address 09h)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
07h	MIN Alarm	AE	MA40	MA20	MA10	MA8	MA4	MA2	MA1
08h	HOUR Alarm	AE	RAM	HA20	HA10	HA8	HA4	HA2	HA1
09h	WEEK Alarm	AE	WA6	WA5	WA4	WA3	WA2	WA1	WA0
	DAY Alarm		RAM	DA20	DA10	DA8	DA4	DA2	DA1

These registers specifies the alarm time using day of the week, day, hour, and minute settings. Address 09h specifies the day of the week or the day setting, selected by the AS (Alarm Select) bit in address 0Bh. The AF (Alarm Flag) bit in address 0Ch is set to "1" when a time is specified in the Alarm Registers.

• Assigning the day of the week using the WEEK Alarm register bits
The WEEK Alarm register WA0 to WA6 bits correspond to the bits in the WEEK register in address 03h: (W4W2W1) = (000) to (110).

Example: When the WEEK register setting for Sunday = (W4W2W1) = (000)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
09h	WEEK Alarm	AE	Sat	Fri	Thu	Wed	Tue	Mon	Sun

The alarm can be set arbitrarily for multiple days of the week.

Example: Monday to Friday alarm, when the WEEK register setting for Sunday = (W4W2W1) = (000)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
09h	WEEK Alarm	0	0	1	1	1	1	1	0

• Minute alarm, hourly alarm, daily alarm function
When the AE (Alarm Enable) bit 7 in a register is set to “1”, the alarm is set to be triggered after every increment (minute, every hour, or every day) of the corresponding register.

Example: Alarm setting for 15 minutes past the hour for every hour

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
07h	MIN Alarm	0	0	0	1	0	1	0	1
08h	HOUR Alarm	1	Don’t care bits when bit 7 = “1”						

• RAM bit
Can be used as a general-purpose RAM bit.

6-4. Timer Counter Register (Address 0Ah)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Ah	Timer Counter	T128	T64	T32	T16	T8	T4	T2	T1

This register specifies the count value of a down-counter used for fixed-cycle timer interrupts.The fixed-cycle timer source clock is specified using the TSS1 and TSS0 (Timer Source Clock Select) bits in address 0Bh. When the TE (Timer Enable) bit in address 0Dh is changed from “0” to “1”, the counter starts counting down from the specified count value. When the down-counter reaches zero, the TF (Timer Flag) bit in address 0Ch is set to “1”. The down-counter continually repeats counting down from the specified count value while the TE bit is “1”.

6-5. Select Register (Address 0Bh)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Bh	Select Register	TCS1	TCS0	CFS1	CFS0	TSS1	TSS0	AS	UTS

• TCS (Temperature Compensation Select) bits
The TCS bits select the temperature compensation, operating interval. Temperature compensation operates in sync with the clock register timing.

TCS1	TCS0	Temperature compensation operating interval
0	0	0.5 s
0	1	2 s
1	0	10 s
1	1	30 s

*When power is applied, TCS is reset to “00” and 0.5 sec temperature compensation operating interval is selected.

• CFS (OUTPUT Frequency Select) bits
The CFS bits select the output frequency

CFS1	CFS0	Output frequency
0	0	32.768 kHz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

* When power is applied, CFS is reset to “00” and 32.768 kHz output frequency is selected.

• TSS (Timer Source Clock Select) bits

The TSS bits select the fixed-cycle timer source clock.

TSS1	TSS0	Timer source clock
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	1/60 Hz

• AS (Alarm Select) bit

The AS bit selects day of week alarm or day alarm. The alarm data in address 09h is interpreted according to the following alarm setting.

AS	Alarm type
0	Day of week alarm
1	Day alarm

• UTS (Update Time Select) bit

The UTS bit selects the timing for generating time update interrupts.

UTS	Time update interrupt timing
0	Seconds digits update
1	Minutes digits update

6-6.Flag Register (Address 0Ch)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Ch	Flag Register	-	-	VDHF	VDLF	-	TF	AF	UTF

• VDHF (Voltage Detect High Flag) bit

The VDHF bit is the temperature compensation operating voltage detection flag.
Voltage detection is performed intermittently in sync with the temperature compensation operating interval timing.

VDHF	Description
0	Supply voltage is VDET1(Max 2.0V) or higher
1	Supply voltage is VDET1(Max 2.0V) or lower

* After detection, the VDHF bit is set to “1” and the value is maintained until you write “0”. Only “0” data can be written to this bit.

• VDLF (Voltage Detect Low Flag) bit

The VDLF bit is the supply voltage under voltage detection and power-ON reset signal detection flag.
Voltage detection is performed intermittently in sync with the temperature compensation operating interval timing.

VDLF	Description
0	Supply voltage is VDET2 (1.5 V max.) or higher, or power-ON reset signal undetected.
1	Supply voltage is VDET2 (1.5 V max.) or lower, or power-ON reset signal detected.

* After detection, the VDLF bit is set to “1” and the value is maintained until you write “0”.Only “0” data can be written to this bit.

• TF (Timer Flag) bit

The TF bit is the fixed-cycle timer interrupt detection flag.

TF	Description
0	Normal operation
1	Fixed-cycle down-counter zero detected

* After detection, the TF bit is set to “1” and the value is maintained until you write “0”. Only “0” data can be written to this bit.

• AF (Alarm Flag) bit

The AF bit is the alarm interrupt detection flag.

AF	Description
0	Normal operation
1	Detects match with alarm set time

* After detection, the AF bit is set to “1” and the value is maintained until you write “0”. Only “0” data can be written to this bit.

• UTF (Update Time Flag) bit

The UTF bit is the time updates interrupt detection flag.

UTF	Description
0	Normal operation
1	Time update completion detected

* After detection, the UTF bit is set to “1” and the value is maintained until you write “0”.Only “0” data can be written to this bit.

6-7. Control Register (Address 0Dh)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Dh	Control Resister	RESET	TEST	RAM	FIE	TE	TIE	AIE	UTIE

• RESET bit

RESET	Description
0	Normal operation
1	1 to 64 Hz frequency divider counter reset. Clock function stops.

• TEST bit

The TEST bit is for manufacturer testing. Leave set to “0” for normal operation.

TEST	Description
0	Normal operation
1	Test mode

• RAM bit

Can be used as a general-purpose RAM bit.

• FIE (Frequency Interrupt Enable) bit
The FIE bit is the enable bit for the 50% duty, 1 Hz signal output on /INT.

FIE	Description
0	/INT 1 Hz output disable
1	/INT 1 Hz output enable

* When power is applied, FIE is reset to “0” and /INT output disable is selected.

• TE (Timer Enable) bit
The TE bit enables the fixed-cycle timer down-counter.

TE	Counter operation
0	Timer count stop
1	Timer count start

* When power is applied, TE is reset to “0” and timer count stop is selected.

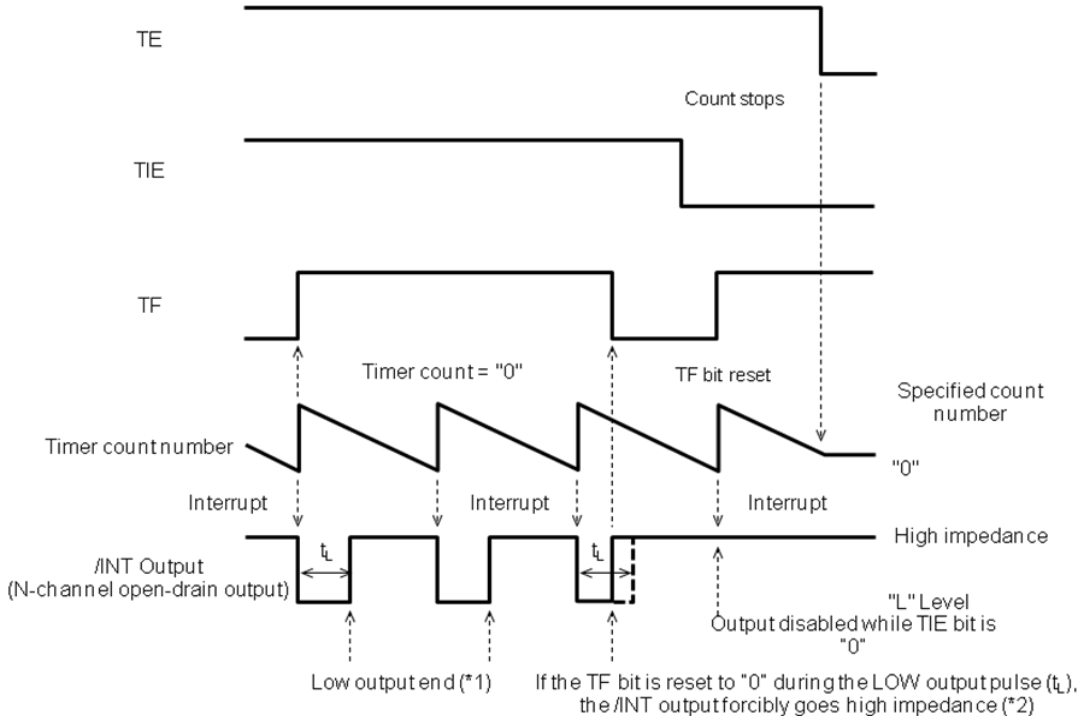
• TIE, AIE, UTIE (Timer, Alarm, Update Time Interrupt Enable) bits The TIE, AIE, and UTIE bits enable the interrupt signal outputs on /INT.TIE controls the fixed-cycle timer interrupt output, AIE controls the alarm interrupt output, and UTIE controls the time update interrupt output.

TIE,AIE,UTIE	Description
0	/INT output disable
1	/INT output enable

* When power is applied, these bits are reset to “0” and /INT output disable is selected. The output from /INT is the logical-OR of the fixed-cycle timer interrupt, alarm interrupt, time update interrupt, and FIE-controlled 1 Hz signal outputs.

7. Interrupt Function Description

7-1. Fixed Cycle Timer Interrupt



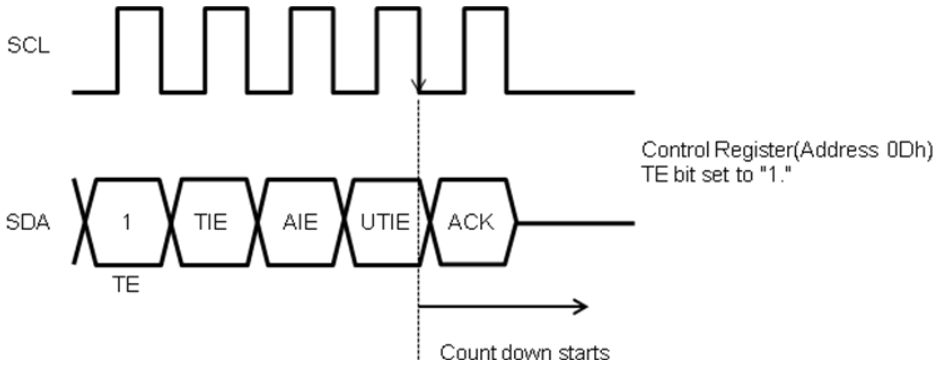
*1: When an interrupt is generated and TIE is “1”, a single Low-level pulse is output on /INT. The pulse width is given below.
*2: If the TF bit is reset to “0” during the /INT LOW-level pulse output after an interrupt, the /INT output immediately stops

TIE	Description
0	/INT fixed-cycle timer interrupt output disable
1	/INT fixed-cycle timer interrupt output enable

* If not using the fixed-cycle timer interrupt function, the timer counter register (Address 0Ah) can be used as general-purpose RAM by setting the TE and TIE bits to “0”.

TSS1	TSS0	Source clock	Low-level output (t_L)
0	0	4096 Hz	0.122 ms
0	1	64 Hz	7.81 ms
1	0	1 Hz	7.81 ms
1	1	1/60 Hz	7.81 ms

• Timer start timing
In write mode, the timer count operation starts from the falling edge of the clock after writing to Address 0Dh, as shown in the following diagram.



• Fixed-cycle timer length
The fixed-cycle timer length is determined by the settings for the timer counter and source clock. Assignable cycle length: 244.14us to 255min
Fixed-cycle timer length =Timer counter set value x *Source clock period
(*: The source clock period is the inverse of the source clock frequency.)

• Example : Register settings for fixed-cycle timer interrupts
For 10-minute fixed-cycle interrupts:

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Ch	-	-	VDHF	VDLF	-	0	AF	UTF
0Dh	RESET	TEST	RAM	FIE	0	0	AIE	UTIE
					TE	TIE		

TF

• Set TF,TE,TIE to “0” to prevent incorrect operation

↓

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Ah	0	0	0	0	1	0	1	0
0Bh	TCS1	TCS0	CFS1	CFS0	1	1	AS	UTS
					TSS1	TSS0		

• Set fixed-cycle timer length
• Set timer count register to 10(0Ah)
• Set source clock to 1 minute (TSS1,TSS0)=(11)

↓

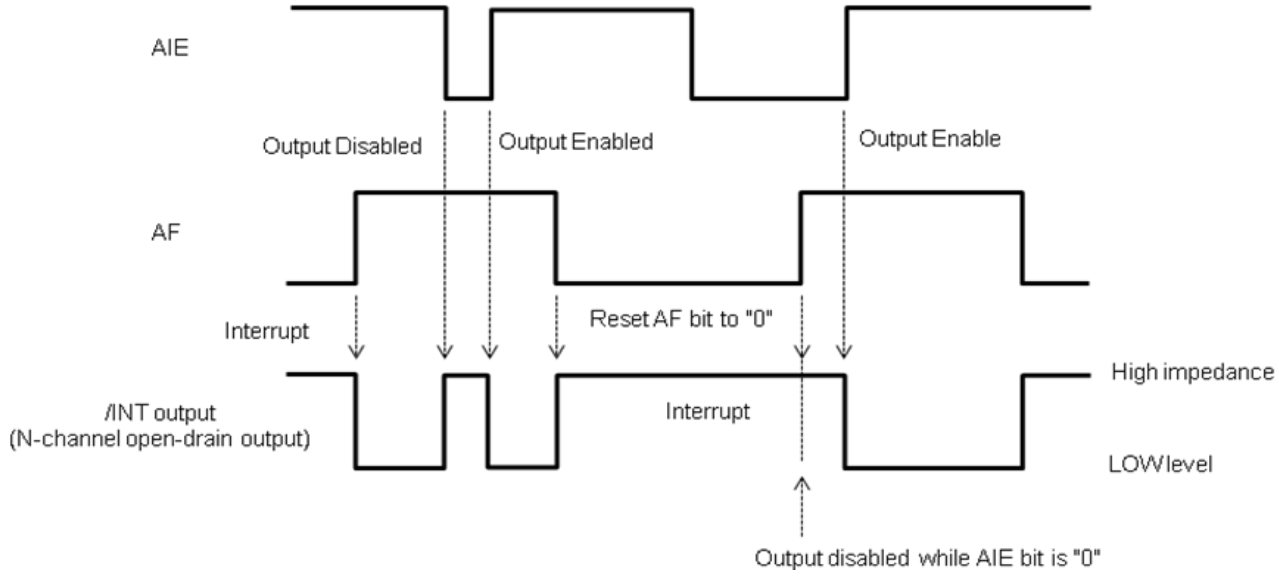
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Dh	RESET	TEST	RAM	FIE	1	1	AIE	UTIE
					TE	TIE		

• Set TE,TIE to “1” to start the timer and enable the /INT output. When the count reaches zero, enters wait state for fixed- cycle timer interrupt

7-2. Alarm Interrupt

The alarm interrupt function generates an interrupt when the clock matches the time setting in the alarm register. When the interrupt is generated, AF is set to “1” and the /INT interrupt signal is output, subject to the state of the AIE alarm interrupt enable bit, as shown in the following diagram.

The alarm interrupt timing occurs when the seconds digits change from 59 seconds to 0 seconds and carries over into the minutes digits.



AIE	Description
0	/INT alarm interrupt output disable
1	/INT alarm interrupt output enable

* If not using the alarm interrupt function, the alarm registers (Address 07h to 09h)can be used as general-purpose RAM by setting AIE bit to “0”.

Example: Register setting for alarm interrupts

For 7:00am alarm from Monday to Friday:

(Assuming the WEEK register (Address 03h) setting for Sunday= (W4W2W1) = (000))

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
0Dh	RESET	TEST	RAM	FIE	TE	TIE	0	UTIE	• Set AIE to "0“ to prevent incorrect operation
							AIE		

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
07h	0	0	0	0	0	0	0	0	• Set the minutes alarm register to 0 minutes (00h)
08h	0	0	0	0	0	1	1	1	• Set the hour alarm register to 7 o’clock (07h)
09h	0	0	1	1	1	1	1	0	• Set the day-of-week alarm register to Monday-Friday (3Eh)
0Bh	TCS1	TCS0	CFS1	CFS0	TSS1	TSS0	0	UTS	• Set AS to “0” to select day-of-week alarm
							AS		

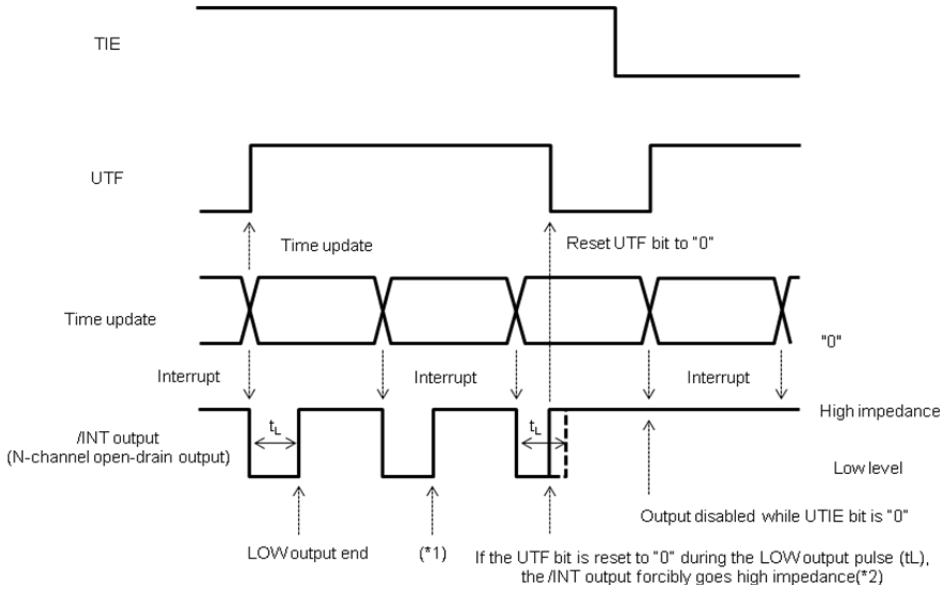
Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
0Ch	-	-	VDHF	VDLF	-	TF	0	UTF	•Reset the AF bit to “0”
							AF		

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
0Dh	RESET	TEST	RAM	FIE	TE	TIE	1	UTIE	•Set AIE to “1” to enable the /INT output. Enters wait state for alarm interrupt
							AIE		

7-3. Time Update Interrupt

The time update interrupt function generates an interrupt whenever the seconds or minutes digits are updated. When the interrupt is generated, UTF is set to “1” and the /INT interrupt signal is output, subject to the state of the UTIE time update interrupt enable bit, as shown in the following diagram. The time update interrupt timing occurs when the digits specified by the UTS bit are updated.

When the RESET bit in Address 0Dh is set to "1“, time update interrupts are not generated.



*1: When an interrupt is generated and UTIE is “1”, a signal LOW-level pulse is output on /INT.The pulse width is given below.

*2: If the UTF bit is reset to “0” during the /INT LOW-level pulse output the /INT output immediately stops. after an interrupt, the /INT output immediately stops.

UTS	Time update timing	LOW-level output (t_L)
0	“Second” update	7.81ms
1	“Minute” update	7.81ms

UTIE	Description
0	/INT time update interrupt output disable
1	/INT time update interrupt output enable

• Example: register settings for time update interrupts.

For time update interrupts when minutes digits are updated.

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Ch	-	-	VDHF	VDLF	-	TF	AF	0
0Dh	RESET	TEST	RAM	FIE	TE	TIE	AIE	0

UTIE

UTF

•Set UTF, UTIE to “0” to prevent incorrect operation

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Ah	TCS1	TCS0	CFS1	CFS0	TSS1	TSS0	AS	1

UTS

•Set time update interrupt
•Set UTS bit to minutes update(1)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Dh	RESET	TEST	RAM	FIE	TE	TIE	AIE	1

UTIE

•Set UTIE to “1” to enable the /INT output. Enters wait state for time update interrupt.

7-4. Interrupt Signal Identification

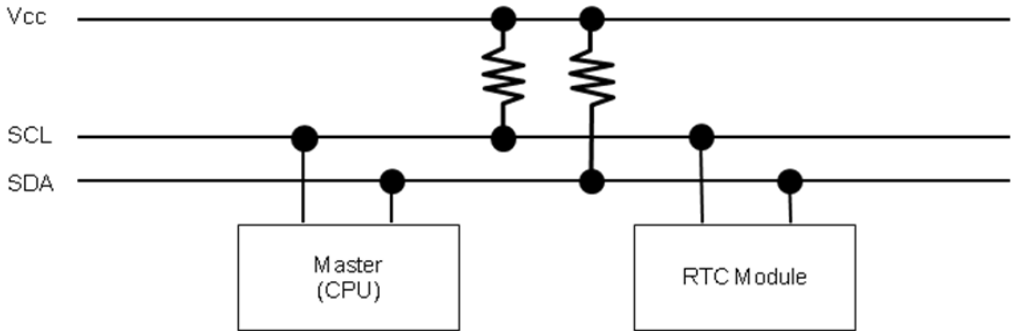
The /INT interrupt output goes LOW when a fixed-cycle timer interrupt, alarm interrupt, or time update interrupt is generated. Whenever an interrupt is generated, the source of the interrupt is indicated by the flags in the flag register (Address 0Ch), so that you can check which interrupt caused the output on /INT.

8. I_2C-BUS Serial Interface

This RTC Module transmits and receives data in the I_2C-BUS serial interface of 2 lines type of SCL (clock line) and SDA (data line).

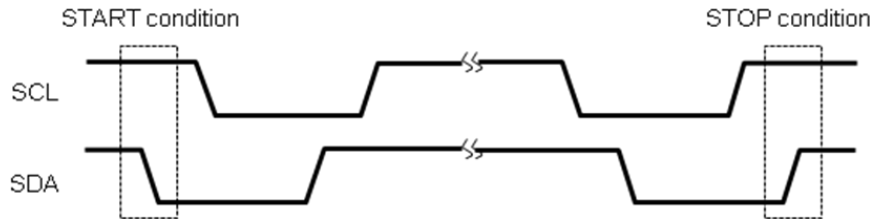
8-1. System Configuration

SCL and SDA are both connected to the VCC line via a pull-up resistance.All ports connected to the I2C bus must be open drain in order to enable AND connections to multiple devices.



8-2. START Condition and STOP Condition

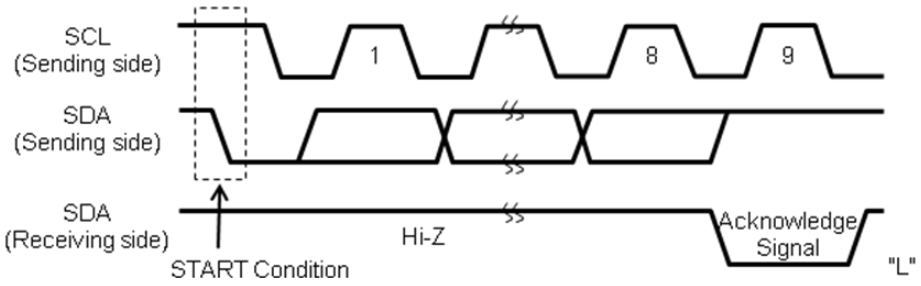
When I_2C-BUS does not perform data transmission, SCL, SDA keep "High".Then SDA varied from High to Low, it becomes the state (START condition), and access is started and performs data transmission. Conversely, SCL is High , that SDA varied from Low to High at the time becomes the state (STOP condition) . The access is end.



8-3. Acknowledge Signal (ACK Signal)

The data transfer is carried out by 8bit START condition after detection. Data to be transferred does not matter how many times each 8bit.Every transfer of 8bit, while the sending and the receiving device, it sends a bit of acknowledgment that the data acknowledge signal.The sending eye on the falling edge of clock pulse and release 8bit (High)the SDA, if the receiver successfully receives the data, and then to Low the SDA. Make sure that the sender is an acknowledge signal comes back by this.Or to send a STOP condition, send the following data.On the other hand, if the receiving side, is recognized as the end of data transfer(RTC module) sending, STOP condition is the master side (do not send an acknowledge signal) not to Low SDA after receiving 8bitby side is the master of the CPU or the like will be transmitted.

Acknowledge signal timing : In case In the case master is the transmission side



8-4. Slave Address

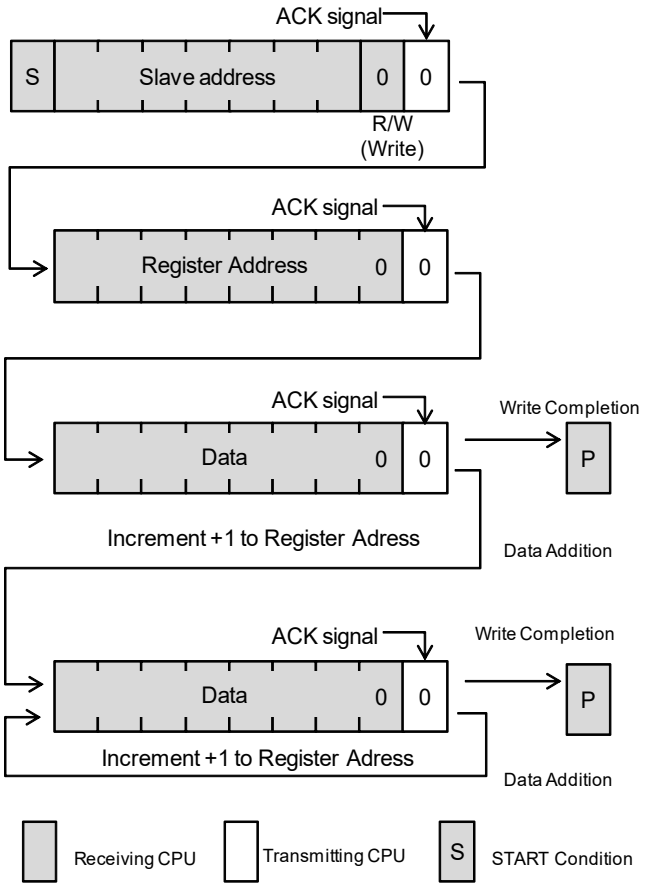
The I_2C-BUS, 7bit slave address has been set for each device. After detecting a START condition, and react to a subsequent communication from the master to be received by the I_2C-BUS slave to this address. When the actual communication, you will receive a 8bit data added along R / W (read / write) bit with the slave address. Slave Address

	Slave address							R/W bit
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write Mode	0	1	1	0	0	1	0	0
Read Mode	0	1	1	0	0	1	0	1

9. I_2C-BUS Data Transfer Sequence

Since the RTC module includes an address auto increment function, it's not necessary to write register address each time. Register address is incremented +1 when 8bit data is transmitted each time. When 0Dh address is incremented +1 , address becomes 00h.

9-1. Data Writing Sequence



•CPU transfers START condition
•CPU transmits the RTC module slave address with the R/W bit set to write mode.
•CPU receives ACK signal from RTC module

•CPU transmits write address to RTC module
•CPU receives ACK signal from RTC module

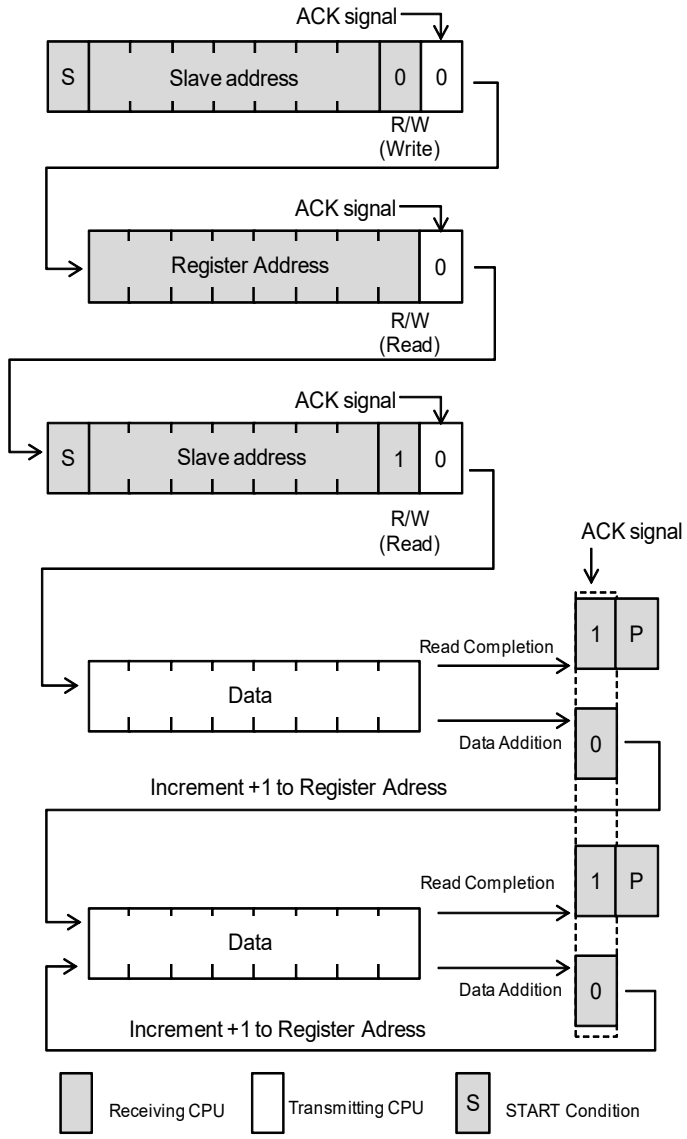
•CPU transfers write data to the address specified as above.
•CPU receives ACK signal from RTC module.
•CPU transmits Stop Condition when written data's finished.

*To transmit data in a row , address data can be written to +1 above If neccesarry to add data.

1.CPU transfers write data to the address which increment +1
2.CPU receives ACK signal from RTC module.
Repeat 1 and 2 above if necessary to add data.
CPU transmits Stop Condition after written data's finished.

9-2. Data Reading Sequence

Data Reading Sequence When Address is specified.



•CPU transfers START condition
•CPU transmits the RTC module's slave address with the R/W bit set to write mode.
•CPU receives ACK signal from RTC module.

•CPU transmits write address to RTC module
•CPU receives ACK signal from RTC module

•CPU retransfers START condition
•CPU transmits the RTC module's slave address with the R/W bit set to write mode.
•CPU receives ACK signal from RTC module

•CPU transfers write data to the address specified as above.
•CPU receives ACK signal from NT3225
•CPU transmits Stop Condition when written data's finished.

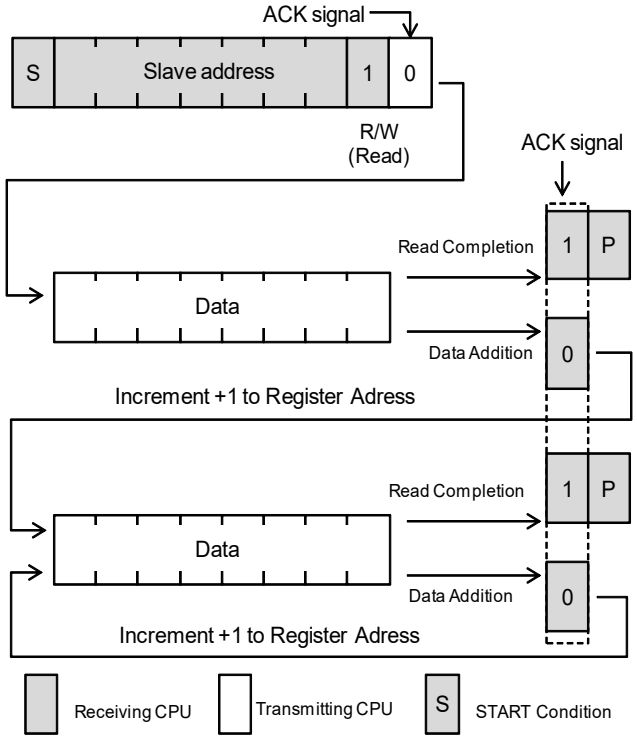
*To receive data in a row , address data can be read as +1 above If neccesarry to add data.

1.CPU transfers ACK signal
2.CPU receives adress data which is added +1 from RTC module.
Repeat 1 and 2 above if necessary to add data.

•CPU doesn't transmits ACK signal after reading data's finished.
•CPU transfers STOP Condition

9-3. Data Reading Sequence When Address is NOT Specified.

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address +1.



•CPU transfers START condition
•CPU transmits the RTC module's slave address with the R/W bit set to write mode.
•CPU receives ACK signal from RTC module.

•CPU does not transmits ACK signal when read copletion.
•CPU transmits STOP Condition

*To receive data in a row , address data can be read as +1 above If neccesarry to add data.

1.CPU transfers ACK signal
2.CPU receives adress data which is added +1 from RTC module.
Repeat 1 and 2 above if necessary to add data.
•CPU doesn't transmits ACK signal after reading data's finished.
•CPU transfers STOP Condition